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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,596	02/12/2004	Gregory J. Fredeman	FIS920040021US1	4927

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,596	FREDEMAN ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,12-18 and 20-24* is/are rejected.

7)☒ Claim(s) *6-11 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Objections

2. Claim 3, 12, 13, and 20-23 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim.

In claim 3, the limitation of "wherein the period of said comparison" contained antecedent problem.

In claim 12 and 22, the limitation of "wherein the time required for allocating a redundancy" contained antecedent problem.

In claim 13 and 23, the limitation of "wherein the time required for allocating a redundancy" contained antecedent problem.

In claim 20, applicant claimed a "fifth transistor" without claim a first to fourth transistor (it is believed that claim 20 is meant to depend on claim 19 and not claim 18).

In claim 21, applicant claimed the "step of maintaining the detection result of said second node", of which contained antecedent problem (it is believed that claim 20 is meant to depend on claim 19 and not claim 18).

Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-5, 12-18, 20-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al, Pat. No. 6320800.

With regard to claim 1, Saito discloses a memory device configured to perform multi-bank operations comprising: a plurality of memory banks (fig. 3, Bank 0, Bank 1) including at least a first (fig. 3, Bank0) and second (fig. 3, Bank1) memory bank respectively controlled by a first (fig. 3, 304 of Bank0) and second (fig. 3, 304 or bank1) redundancy replacement means; and means (fig. 4A, 313a) for comparing data bits read out from said first memory bank (fig. 4A, assuming Bank0 is selected for reading) against corresponding expected data (fig. 4A, from 312) said comparison occurring only when said first bank is addressed during a multi-bank operation (assuming bank0 is selected for reading) (col. 11, line 47-50) (also with regard to claim 5).

With regard to claim 2, Saito discloses further second means (fig. 4A, 313b) for comparing the data bits read out of the second memory bank (while Bank0 is selected for reading, Bank1 is selected for writing) against corresponding expected data (fig. 4A, 312) (col. 11, line 66-col. 12, line 7).

With regard to claim 3, Saito inherently disclosed wherein the period of said comparison is longer than the bank-to-bank access cycle time of the multi-bank operation (the operating time is naturally would take longer to conduct the comparison operation than it would to just accessing the bank-to-bank operation.) (also with regard to claim 12 and 13).

With regard to claim 4, Saito discloses wherein said means (fig. 3, 315) selects either the first or the second bank to perform said comparison and wherein said comparison is enable only when the selected bank is address (col. 10, line 30-36).

With regard to claim 14, Saito discloses further means for fetching address bits only when comparing means compares data bits read out from said memory bank against corresponding expected data (fig. 4A, HITa<0:15>, HITb<0:15>) (col. 11, line 47-65).

With regard to claim 15, Saito discloses a memory device configured to perform multi-bank operations comprising: a plurality of memory banks (fig. 3, Bank0, Bank1) wherein at least two banks are supported by separate redundancy replacement means (fig. 3, 304 of Bank0, 304 of Bank1); identifying means for identifying one bank of said plurality of memory banks (fig. 3, 315); a comparison means (fig. 4A, 313a, 313b); enabling means (fig. 4A, Address buffer

corresponding to Address command indicating that the operation is read operation, and 310 corresponded to command that indicate write or erase operation) for enabling at least two of said banks in a multi-bank mode (Bank0 can operate the read while Bank1 operates in the write or erase operation), for accepting expected data, and for generating an enable signal, wherein said enabling means enables said comparison means (enable by the signal 305a or 305b) to detect if data bits read from one of said bank matches its expected data only when said identification means identifies said corresponding bank during said multi-bank operation.

With regard to claim 16, Saito discloses further an address storage means (fig. 4a, 307 for storing read address, 308 for storing write address or 309 for storing erase address) for storing address bits therein only when said identification means identifies a predetermined bank during the multi-bank operation.

With regard to claim 17, Saito discloses further a plurality of address registers, each of which supports corresponding banks (fig. 4a, 307, 308, 309); means for enabling a redundancy allocation to a predetermined memory bank during said multi-bank operation (fig. 4A, HITb,<0:15>, HITa,<0:15>); means for switching said redundancy allocation to another of said memory banks and for switching an address register to said another memory bank (fig. 4B, 317a, 317b) (col. 12, line 48-054); means for enabling the redundancy allocation to all of said memory banks during the multi-bank operation by applying an addressing pattern

to all of said memory banks during the multi-bank operation (fig. 4B, 324a-324c) (col. 12, line 55-col. 13, line 3).

Drafted as Method claim

4. As per claim 18-24 encompass the same scope of invention as to that of claim 1-17 except they are draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Allowable Subject Matter

5. Claim 6-11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not show in combination with other features, the interconnection of the comparison means being a dynamic exclusive OR circuit comprising: a first transistor coupled to the data, to a first node, and to a second node, a second transistor coupled to the complement of the expected data, to a first voltage source, and to said first node, a third transistor coupled to the complement of said data, to a third node, and to the second node, and a fourth transistor coupled to the expected data, to the first voltage source, and to the third node, such that the second node follows the first voltage source only if no match of the data to the expected data occurs.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Abe (5293348), Ghassemi et al (6757852) and Taura et al (6707733) disclose a memory device having redundancy memory cells.

7. When responding to the office action, Applicants□ are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

July 2005

CONNIE C. YOHA
PRIMARY EXAMINER